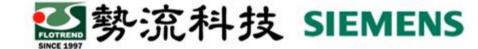




### Flotherm XT 2210功能介紹

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- ② CAE Division/CAE Engineer
- ethan@flotrend.com.tw





### Outline

EDA Bridge

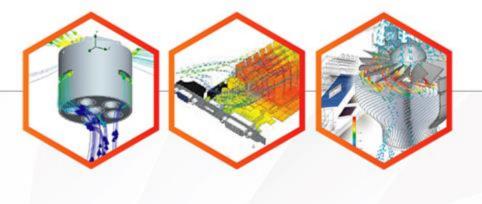
HyperLynx PI Co-Simulation

Parametric study





# **EDA** Bridge





### Solder Mask Import

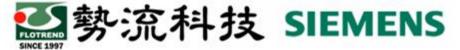
#### Challenge:

PCB的solder mask層在熱分析中經常被忽略,為確保在PCB在3D模型端的總高且PCB內各層能平滑的過渡將solder mask層詳細模型納入模擬是必要的

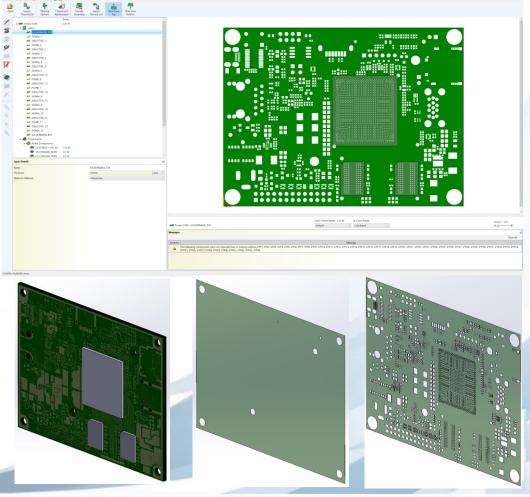
#### Solution:

可以選擇匯入或建立solder mask,並匯入Flotherm XT中

- 有兩種模型可以編輯Solder Mask
  - Simple 只有板上的孔
  - Explicit —包含pin的孔
- Thermal Territories須獨立設定



#### 能得到PCB更高的精確度



### 警勢流科技 SIEMENS

### Solder Mask 進入流程的優化

#### Process to include solder mask.

Version 2021.2

Import & transfer EDA File using EDA Bridge (no solder mask)

Create a new part (top solder mask)

Sketch outline of board including holes (use board as reference)

Extrude to appropriate thickness

Repeat for bottom solder mask

Run simulation

Version 2210

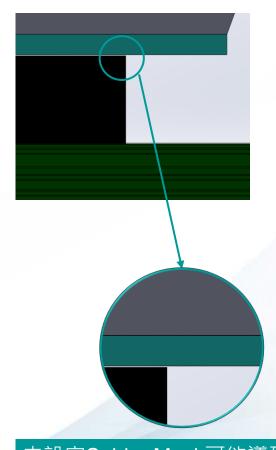
Import & transfer EDA File using EDA Bridge (solder mask is included)

Manual steps avoided

Manual steps avoided

Run simulation

舊版本(V2021.2)要建立 Solder Mask層需在3D端建 立草繪再長料產生模型 新版本(V2210)可直接匯入包含Solder Mask資訊的檔案,可直接匯入到Flotherm XT介面進行模擬



未設定Solder Mask可能導致 在模型產生極小的間隙



### Pin and Via groups

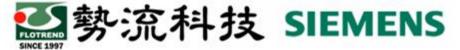
#### Challenge:

如要編輯數十到數百的pins跟vias,在選擇過程非常耗費時間且很容易發生失誤

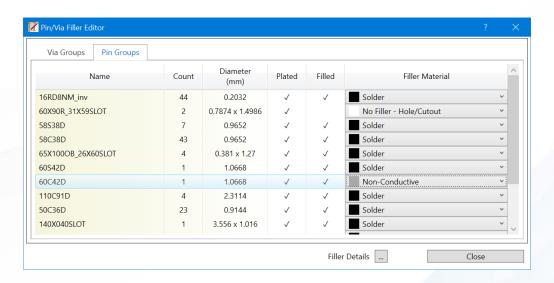
#### Solution:

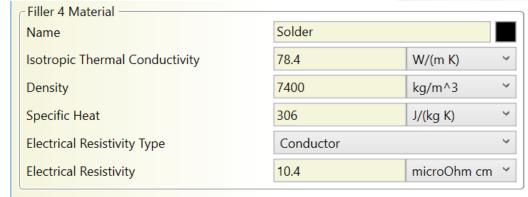
新增Pin/Via Editor 來群組式管理及定義材料參數,功能如下:

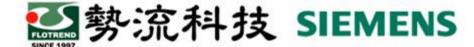
- Pin/Via群組資訊的顯示
- 使用者可定義Pin/Via群組的材料參數
- 可轉換成以下兩種模式
  - Explicit Nets or Thermal Territories



#### 讓編輯PCB資訊更快速且更容易



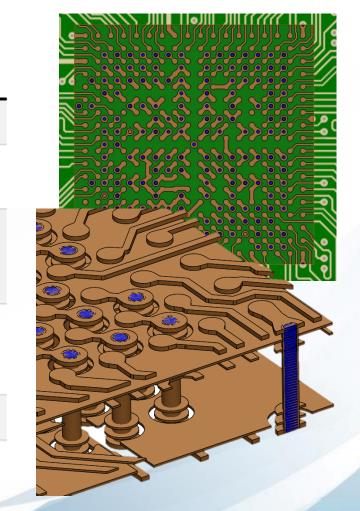




# Pin and Via groups

#### Process to change Pin/Via filler

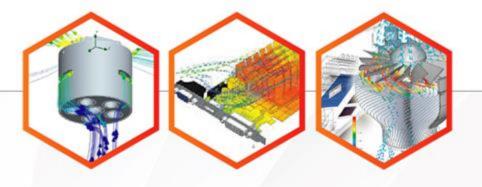
| Version 2021.2  | Version 2210  |
|---|---|
| Import EDA File using EDA Bridge  | Import an EDA File using EDA Bridge                 |
| Export areas of the board that have pins and vias using explicit modeling | Edit the materials in the Pin and via Filler editor |
| Individually select the (100s-1000s) pins and vias to apply materials     |   |
| Run simulation  | Run simulation                                      |
| 舊版本(V2021.2)在選擇<br>Pins/Vias時會花費較多的時                                      | 新版本(V2210)可以在Pin/Via<br>Editor設定材料參數                |







## HyperLynx PI Co-Simulation





### Thermal Co-Simulation

#### Challenge:

在HyperLynx DC Drop 的模擬中·結果無法可視 化

#### Solution:

能產生DC Drop結果報告

#### Challenge:

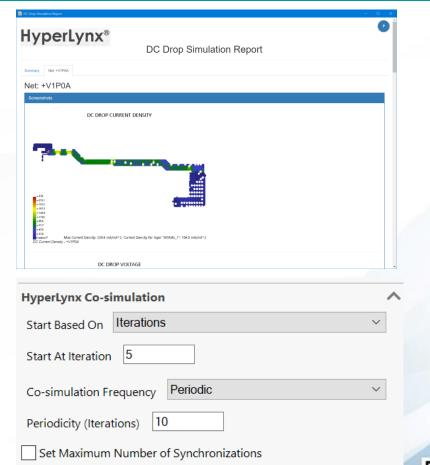
在先前的Co-simulation,為了精準度,每次迭代計算後HyperLynx的功率與Flotherm XT的溫度不會同步,但增加了計算時間

#### Solution:

新增Co-simulatio的設定選項,可以設定 HyperLynx的功率與Flotherm XT的溫度模擬的同 步頻率



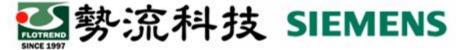
#### 能更快的得到模擬結果



✓ Create HyperLynx Report

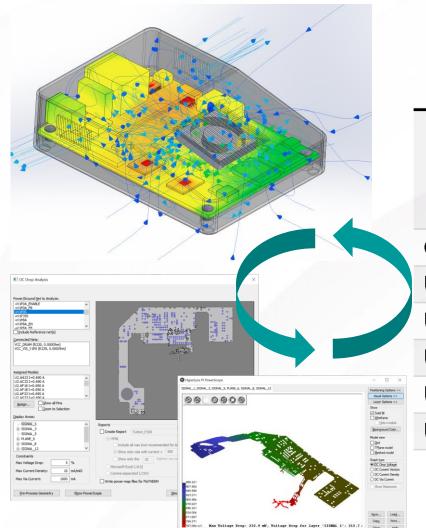


### Thermal Co-Simulation



Run B

#### 設定Co-simulation同步頻率,可降 低20%的計算時間



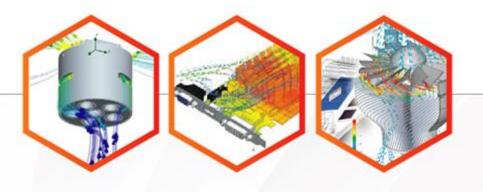
|                          | HyperLynx Co-simulation  Start Based On Iterations   Start At Iteration 0  Co-simulation Frequency Each Iteration   Create HyperLynx Report | Co-simulation Frequency Periodic |
|--------------------------|---|----------------------------------|
| CPU time (s)             | 10116   | 799620%                          |
| U16 Die Temperature (°C) | 73.57   | 73.56                            |
| U17 Die Temperature (°C) | 72.19   | 72.18                            |
| U18 Die Temperature (°C) | 74.77   | 74.76                            |
| U19 Die Temperature (°C) | 73.92   | 73.92                            |
| U20 Die Temperature (°C) | 76.80   | 76.79                            |

Run A





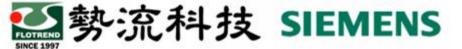
### Parametric study





### Parametric study

- 新增匯出專案功能(包含parametric study設定),可選擇包含結果或不包 含結果,位置於Project Tools下(Fig. A)
- 新增能對單一scenario匯出功能,可 選擇包含結果或不包含結果(Fig. B)



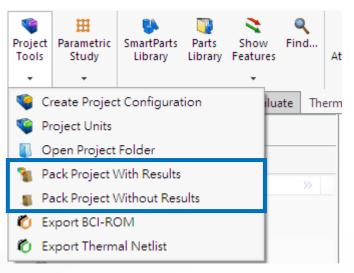


Fig. A

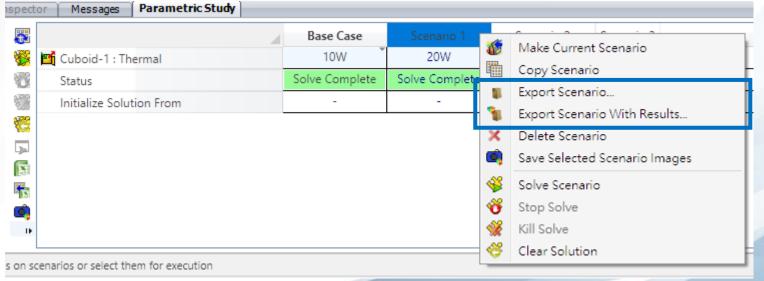
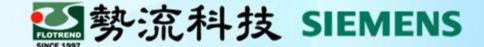
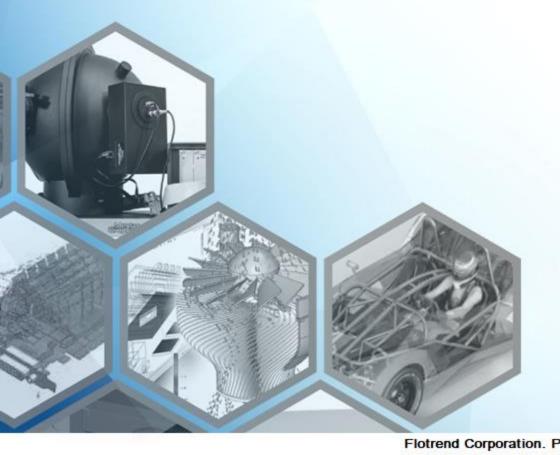




Fig. B



# Thank you for your attention.



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